

Semiconductor Packaging & Testing Market Research

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For and on behalf of
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Frost & Sullivan

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Agenda

- 1 Introduction of the Research
- 2 Overview of Semiconductor Market
- 3 Overview of Packaging & Testing Market
- 4 Overview of Advanced Packaging Market
- 5 Competitive Landscape of Packaging & Testing Market
- 6 Appendix

Scope

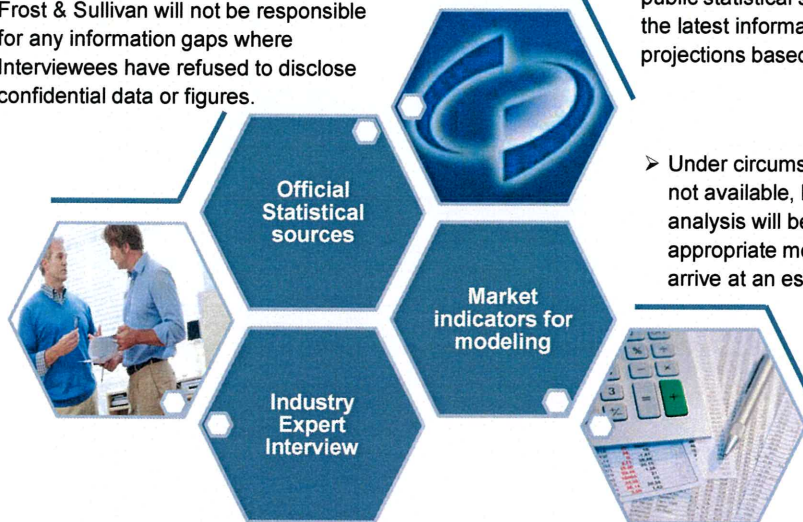
■ The project scope is defined as follows:

Research Period	<ul style="list-style-type: none">• Historical Year: 2020-2025• Base Year: 2025• Forecast Year: 2025-2030E
Geographic Scope	<ul style="list-style-type: none">• Global• China
Industry Scope	<ul style="list-style-type: none">• Semiconductor Market• Packaging & Testing Market• Advanced Packaging & Testing Market

Limitations

■ Source of Information

- Interviews with industry experts and competitors will be conducted on a best-effort basis to collect information in aiding in-depth analysis for this report.
- Frost & Sullivan will not be responsible for any information gaps where interviewees have refused to disclose confidential data or figures.



- The study took 2025 as the base year and 2025-2030 as the forecast period. However, as the point of this study being 2026, some of the figures of 2026 may not be available at the moment from public statistical sources. Frost & Sullivan will use the latest information available (e.g. 2025) or make projections based on historical trends.

- Under circumstances where information is not available, Frost & Sullivan in-house analysis will be leveraged using appropriate models and indicators to arrive at an estimate.

- Source of information will be stated in the right hand corner at the bottom on each slide for easy reference.

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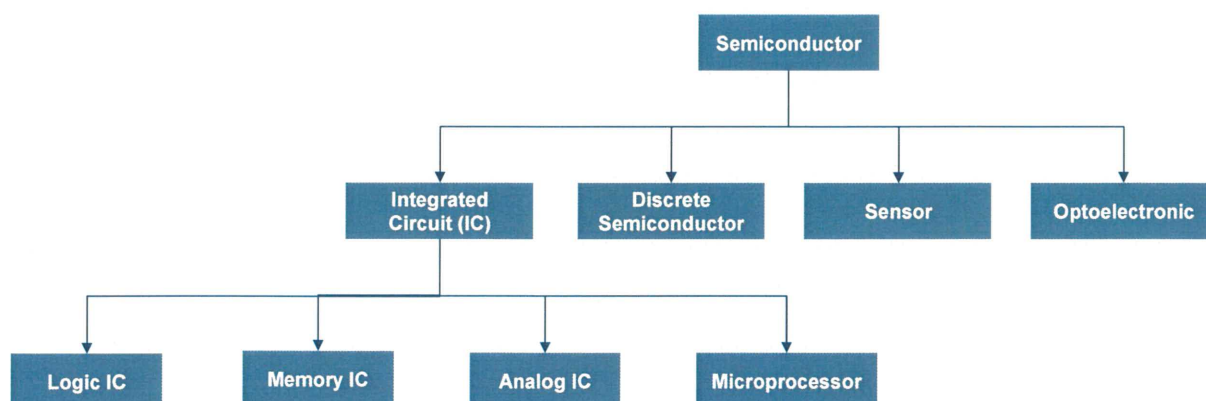
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Overview of Global Semiconductor Market

Definition and Categorization of Semiconductor

The semiconductor product landscape is highly diverse, broadly categorized into integrated circuits (ICs), discrete devices, optoelectronic devices, and sensors.

Integrated circuits, commonly referred to as "chips," are functional circuits formed by integrating a specific number of components and their interconnections through semiconductor manufacturing processes. They can be further subdivided into logic circuits, memory, microprocessors, and analog circuits, among which logic circuits and memory hold the largest market shares.



Overview of Global Semiconductor Market

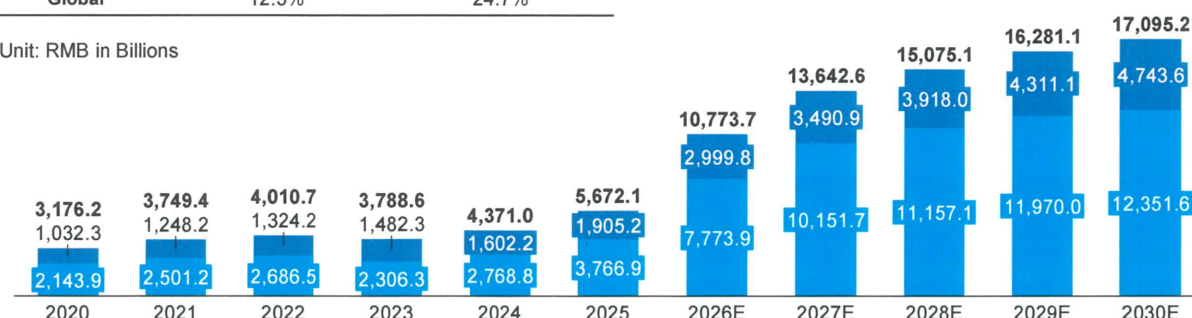
China Semiconductor Market Size Analysis

The semiconductor market boasts immense scale and broad prospects. As the global economy evolves and technological innovation advances, semiconductors—recognized as the core of the information technology and electronics industries—are growing increasingly vital. The rapid development of emerging technologies such as AI, 5G, the Internet of Things (IoT), and automotive electronics has spurred robust demand for high-performance, low-power consumption chips, driving sustained growth in the semiconductor market. In 2025, the global and Chinese mainland semiconductor markets size reached RMB5,672.1 billion and RMB1,905.2 billion respectively; it is projected that by 2030, these global and Chinese mainland semiconductor markets size will grow to RMB17,095.2 billion and RMB4,743.6 billion.

Global and China Semiconductor Market Size

CAGR	2020-2025	2025-2030E
PRC*	13.0%	20.0%
Rest of the World	11.9%	26.8%
Global	12.3%	24.7%

Unit: RMB in Billions

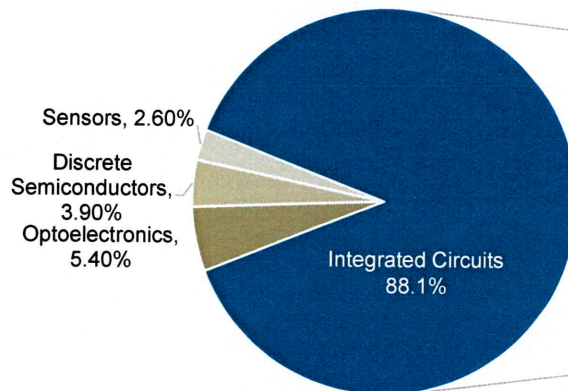


Overview of Global Semiconductor Market

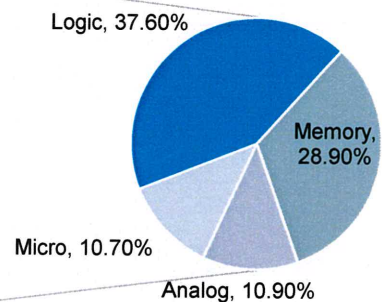
Market Breakdown of Global Semiconductor Market

In 2025, the global semiconductor market reached a total value of RMB 5,672.1 billion. The market was overwhelmingly dominated by Integrated Circuits, representing approximately 88.1% of the entire market. Within the Integrated Circuits segment, Logic was the largest category, followed by Memory. Analog and Micro components held smaller shares, respectively.

Market Breakdown of Global Semiconductor Market, by Category, 2025



Market Breakdown of Integrated Circuits Market, by Type, 2025



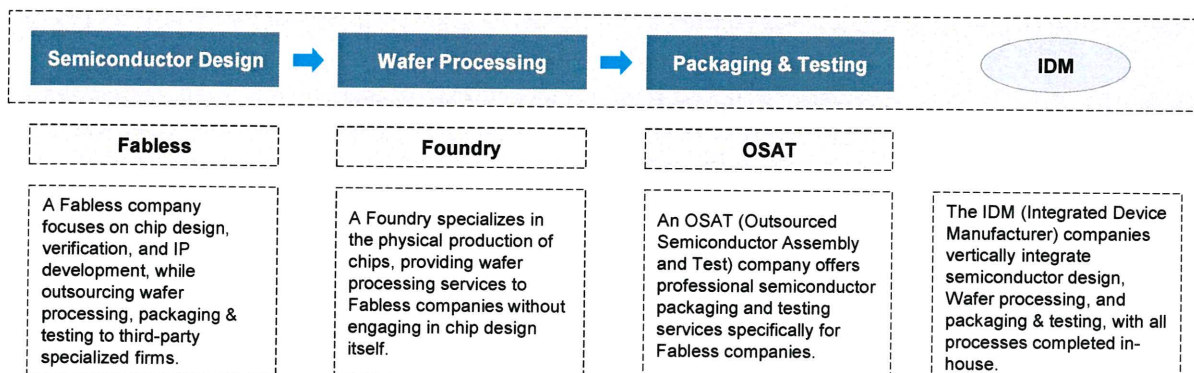
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Overview of Global Semiconductor Market

Analysis of Key Segments and Business Models in Semiconductor Industry (1/2)

The semiconductor industry chain primarily consists of three core segments: chip design, wafer processing, and packaging & testing. Based on the level of involvement in these segments, the semiconductor industry encompasses various business models, including Fabless, Foundry, OSAT, and IDM.



As the semiconductor industry evolves, the resources required for each segment have grown significantly. This has driven the further deepening of vertical specialization, emerging as a key trend in the industry's development. While traditional semiconductor giants maintain a certain degree of IDM operations, more semiconductor companies are adopting the Fabless model to allocate greater resources to complex chip design. Against this backdrop, an increasing share of packaging and testing work is being outsourced to specialized third parties, creating favorable growth opportunities for OSATs.

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Overview of Global Semiconductor Market

Analysis of Key Segments and Business Models in Semiconductor Industry (2/2)

Model	Advantages	Disadvantages
Fabless	<ul style="list-style-type: none"> Low capital investment, high capital turnover efficiency, and strong anti-cyclical risk capability; Focus on design enables rapid innovation and quick response to market changes; No need to bear manufacturing equipment depreciation or process iteration costs. 	<ul style="list-style-type: none"> Dependent on external manufacturing and packaging resources, with supply chain stability constrained by Foundry and OSAT capacities; Weak control over manufacturing process details, potentially affecting product performance optimization; Profit sharing with Foundry required, with costs subject to foundry price fluctuations.
Foundry	<ul style="list-style-type: none"> High professional expertise in manufacturing processes, significant economies of scale, and low unit manufacturing costs; Focus on process R&D enables rapid technological iteration (e.g., breakthroughs in advanced nodes); Diversified customer base reduces reliance on single market risks. 	<ul style="list-style-type: none"> Enormous initial investment (single fab costs billions to tens of billions of dollars) with high depreciation pressure; Rapid technological iteration requires continuous R&D investment to maintain competitiveness, with risk of customer loss if falling behind; Profitability affected by capacity utilization fluctuations (e.g., equipment idling during demand downturns).
OSAT	<ul style="list-style-type: none"> Professional packaging and testing technologies, capable of providing diverse packaging solutions; Flexible production capacity that can be adjusted according to customer needs, with high service efficiency; Lower capital investment compared to Foundry, with relatively lower barriers to capacity expansion. 	<ul style="list-style-type: none"> Intense industry competition, with price wars potentially compressing profits; Technological dependence on upstream sectors (e.g., packaging materials, equipment) limits innovation space; Order volume directly affected by customer demand fluctuations (e.g., order cuts from chip design companies).
IDM	<ul style="list-style-type: none"> Full-process collaborative optimization, with deep matching between design and manufacturing processes ensuring more stable product performance; Self-controllable supply chain, not restricted by external capacity constraints (e.g., ensuring supply during chip shortages); Profound long-term technological accumulation, suitable for customized, high-barrier chips (e.g., power semiconductors, analog chips). 	<ul style="list-style-type: none"> Excessively heavy assets with huge capital expenditure and high R&D and equipment depreciation pressure; Low business flexibility with high costs for transformation or product direction adjustment (e.g., asset losses when abandoning old processes); Weaker economies of scale compared to specialized Foundry/OSAT, with potential lower efficiency in individual links than specialized division models.

Overview of Global Semiconductor Market

Drivers and Trends of Global Semiconductor Market

Strong Demand from Diverse Downstream Applications

Sustained demand surges in downstream sectors — including consumer electronics, smart manufacturing, new energy vehicles, and data centers — are expanding the semiconductor market. Smart terminal upgrades drive demand for high-end chips; industrial automation boosts industrial-grade semiconductors; rising in-vehicle electronics penetration increases automotive-grade semiconductor consumption; and exponential computing power needs expand the server chip market. These diverse scenarios accelerate semiconductor product iteration, promote upstream-downstream capacity coordination and tech innovation, and form a positive demand-driven growth cycle.

Technology Iteration Toward Process Nodes and Packaging

Semiconductor manufacturing processes are breaking through to 5nm, 3nm, and beyond, while advanced packaging has become a key path to enhance performance. Advanced nodes improve chip computing density, and advanced packaging optimizes system energy efficiency via heterogeneous integration — these two technologies synergize to meet high-end application needs. Tech upgrades drive innovation in upstream links (e.g., equipment, materials), accelerate industrial chain resource concentration in high-value-added segments, and push enterprises to increase R&D investment to seize technological leadership.

National Policy Support Drives Localization of the Industrial Chain

Countries worldwide are strengthening semiconductor industry support policies. Domestically, measures like subsidies and R&D incentives optimize industrial chain layout. Driven by these policies, localization of key links (chip design, manufacturing, equipment) has accelerated, and local enterprises' market share has gradually risen. Policy dividends attract capital and talent, promote upstream-downstream coordinated development, and enhance supply chain self-reliance and international competitiveness.

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Overview of Global Semiconductor Packaging & Testing Market

Introduction to Semiconductor Packaging & Testing Industry Chain

Semiconductor Packaging refers to the process of encapsulating manufactured semiconductor bare dies or wafers into protective casings through a series of technological procedures. This process provides functions such as physical protection, electrical connection, and thermal management, enabling them to become independent devices applicable to various electronic equipment. Semiconductor Testing refers to the process of detecting the electrical performance, functional integrity, reliability, and environmental adaptability of semiconductors using professional testing equipment, so as to screen out qualified products and eliminate defective ones.

Overview of Global Semiconductor Packaging & Testing Market

Technical Requirements for Semiconductor Packaging

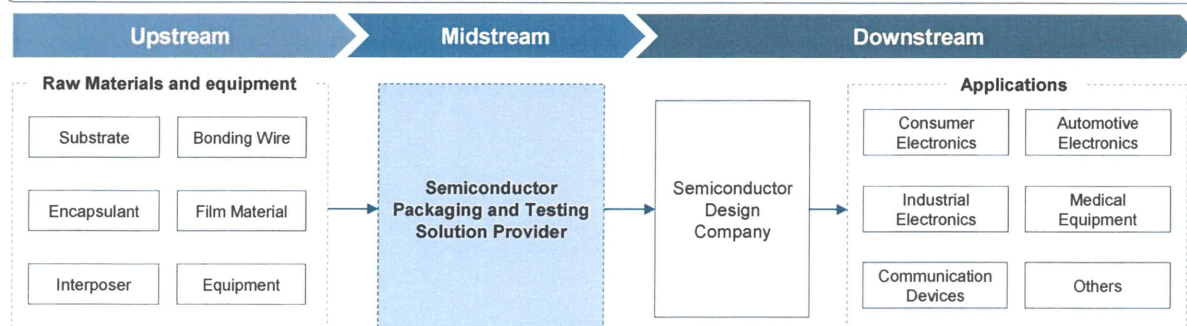
- The development of the microelectronics industry has imposed new requirements on packaging technology. With the rapid advancement of integrated circuits (ICs), an increasing number of functions must be embedded within a single chip, raising integration standards. In parallel, miniaturization has become a key trend to meet demands for portability and compact design. As a result, IC packaging faces ever-higher technical requirements.

Technical Requirements	Specific Requirements
Miniaturization	Packaging continues to evolve toward ultra-compact formats, including wafer-level packaging (WLP) where the package size equals the chip size. Achieving miniaturization requires low cost, high quality, short lead time, and compliance with international form-factor standards.
Thermal management	As IC power consumption rises, smaller package dimensions increase thermal resistance. Complex operating environments demand effective heat dissipation solutions to ensure stability and reliability under prolonged high-temperature operation. Ultimately, semiconductor progress depends on reducing power consumption, with low-power design remaining a critical breakthrough.
Higher integration	To support larger chips, packaging may adopt low-stress die-attach materials, low-stress transfer molding compounds, or wave-sealed resins to mitigate stress transfer.
High density	Greater functional integration requires packages with higher pin counts and tighter spacing, significantly increasing design and manufacturing complexity.
Multi-lead adaptation	The growing number of external leads poses challenges, as lead spacing cannot shrink indefinitely (below ~0.5 mm), or soldering reliability during reflow deteriorates. Multi-lead packages such as Tape Carrier Package (TCP) and Ball Grid Array (BGA) are becoming mainstream solutions.
High-temperature reliability	At elevated temperatures, Au/Al bond interfaces may degrade due to halogen compounds released from brominated epoxy molding resins, causing voids, increased resistance, or even disconnection. Alternative flame-retardant materials are under development.
High reliability	Stable performance, reliability, and long service life are essential, particularly for ICs. While metal and ceramic packages already meet stringent military standards, their high cost limits widespread adoption.
Environmental compliance	Environmental concerns focus on lead dissolution from discarded products causing acid rain, groundwater contamination, and health hazards, as well as halogenated resins releasing harmful byproducts. Lead-free solders, with their higher melting points, demand stricter thermal resistance from semiconductor components and packages.

Overview of Global Semiconductor Packaging & Testing Market

Introduction to Semiconductor Packaging & Testing Industry Chain

- The semiconductor packaging and testing industry chain consists of several key segments. In the upstream, raw materials including substrates, bonding wires, encapsulants, bumping materials, interposer, and equipment serve as the foundational input. The midstream features semiconductor packaging and testing solution providers that leverage these upstream raw materials to offer specialized packaging and testing services. This requires them to possess profound expertise in complex packaging technologies, precision testing methodologies, and material science. These packaged and tested products then supply semiconductor design companies. The downstream encompasses a wide range of applications, such as consumer electronics, automotive electronics, industrial electronics, medical equipment, communication devices, and other fields.



Testing and Assembly companies (OSATs) can provide customers with customized, comprehensive testing and assembly technology solutions, and they are positioned in the midstream of the semiconductor industry chain. The workflow is as follows: Semiconductor design companies (Fabless) entrust wafer foundries (Foundry) to deliver the manufactured wafers to OSATs. In accordance with the technical standards agreed with the Fabless companies, OSATs design testing and assembly solutions, conduct processes such as wafer packaging and testing on the wafers, and then transfer the processed wafers to downstream manufacturers designated by customers for the subsequent manufacturing of end products. Primarily, OSAT companies generate revenue and profits by offering packaging and testing services.

Overview of Global Semiconductor Packaging & Testing Market

Development Stages of Semiconductor Packaging & Testing

Stage	Explanation	Representative Technology
Stage #1	Dominated by Dual In-line Packages (DIP) with through-hole pin mounting on PCBs; limited density and frequency hindered automation.	TO; DIP
Stage #2	Pins were replaced by surface-mounted leads, with formats such as Plastic Leaded Chip carrier (PLCC), Small Outline Package (SOP), Small Outline Package (SOP) and QFP (Quad Flat Package).	SOT; SOP; PLCC; QFP
Stage #3	Advanced lead-free packaging technologies emerged, represented by Ball Grid Array (BGA), Wafer-Level Packaging (WLP), and enabling smaller form factors and enhanced system performance.	QFN; BGA; WLP
Stage #4	A wave of new approaches appeared, including System-in-Package (SiP), bumping.	MCM; SiP; Bumping
Stage #5	Further innovations such as Flip-Chip (FC), and Through-Silicon Via (TSV) technology were introduced.	2.5D/3D; MEMS; TSV; FC; Fan-out

Overview of Global Semiconductor Packaging & Testing Market

Global Semiconductor Packaging & Testing Market Size (1/2)

- The global semiconductor market boasts enormous potential and vast space. Spurred by the vigorous development of fields like consumer electronics, automotive electronics, and industrial control, which boosted the demand for semiconductors, the global semiconductor packaging and testing market increase from RMB495.6 billion to RMB804.8 billion with a CAGR of 10.2% from 2020 to 2025. During this period, Chinese Mainland market achieved a market size of RMB314.4 billion in 2025, with a CAGR of 12.4% from 2020 to 2025, outpaced the rest of the world that had a CAGR of 8.9%.
- Looking ahead, the global semiconductor market is expected to grow to RMB1,383.1 billion by 2030 at a faster rate, with a global CAGR of 11.4%. This growth is driven by the accelerating digital transformation, the expansion of automotive electrification, and the continuous progress of artificial intelligence, all of which will drive a surge in demand for semiconductors. Chinese Mainland market is projected to maintain strong growth momentum and will reach RMB598.2 billion by 2030 with a CAGR of 13.7% from 2025 to 2030. Meanwhile, the Chinese Mainland share in the global market continues to rise, reflecting the country's growing significance in the semiconductor packaging and testing industry amid these favorable industrial drivers.

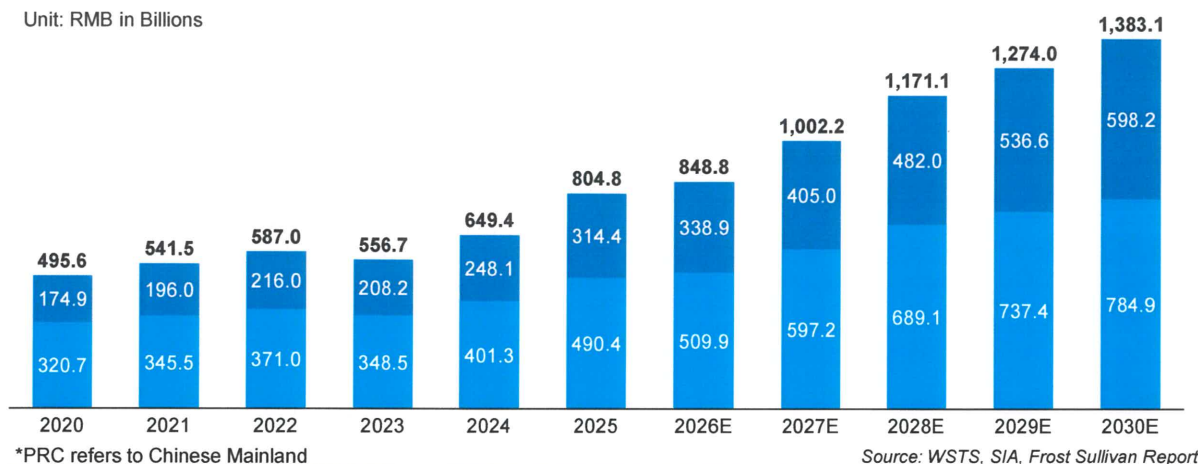
Overview of Global Semiconductor Packaging & Testing Market

Global Semiconductor Packaging & Testing Market Size (2/2)

Global and China Semiconductor Packaging & Testing Market Size

	CAGR	2020-2025	2025-2030E
PRC*		12.4%	13.7%
Rest of the World		8.9%	9.9%
Global		10.2%	11.4%

Unit: RMB in Billions



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Overview of Global Semiconductor Packaging & Testing Market

Drivers and Trends of Semiconductor Packaging & Testing Industry



The Growth of Semiconductors Drives the Expansion of the Packaging & Testing Industry

The demand for semiconductors has surged across multiple fields such as consumer electronics and automotive electronics. Technologies like 5G and AI have spurred the demand for high-performance chips, fueling the expansion of the semiconductor market. This provides a steady stream of orders for the packaging and testing industry, whose market scale has grown steadily in tandem with the semiconductor sector and is expected to maintain a high growth rate in the future.



Bottlenecks in Process Miniaturization Drive the Development of Advanced Packaging

As chip process nodes shrink to 7nm, 5nm, and beyond, they face physical and cost challenges — making advanced packaging a key breakthrough. Technologies including 2.5D/3D packaging and Chiplet enhance chip performance and integration while reducing costs through innovative interconnection and integration solutions, thereby driving technological innovation and value enhancement in the packaging and testing industry.



OSATs Strengthen Collaboration with Upstream and Downstream Sectors

With the refinement of industrial division of labor, OSATs (Outsourced Semiconductor Assembly and Testing companies) have deepened collaboration with upstream and downstream partners. They jointly optimize designs with Fabless companies to provide customized solutions for downstream clients, and work with Foundries to ensure smooth workflow. These efforts collectively promote the development of packaging industry, improve packaging efficiency and quality, and enhance the overall competitiveness of the industrial chain.

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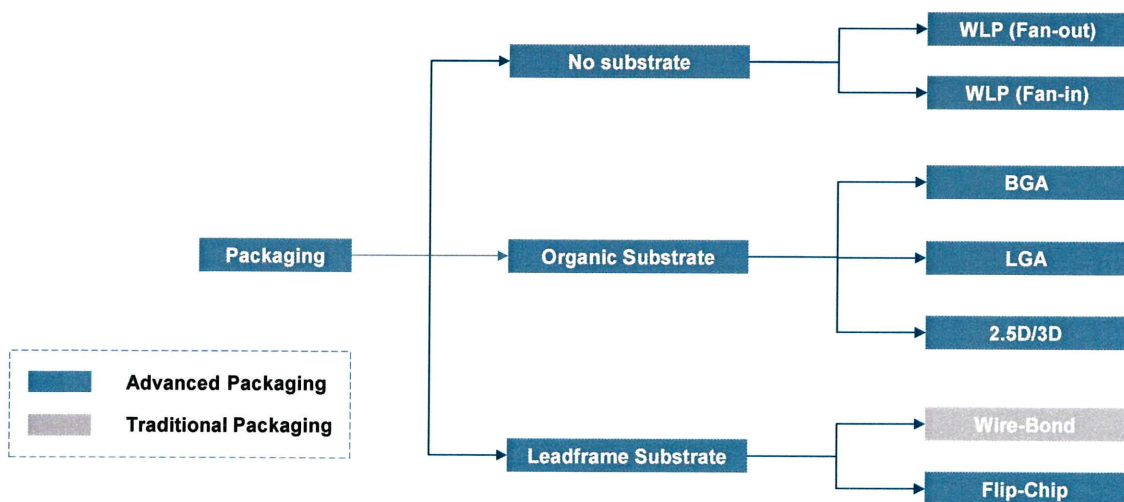
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Overview of Global Advanced Packaging & Testing Market

Definition and Classification of Semiconductor Advanced Packaging

- Advanced packaging refers to a packaging solution with process complexity, achieved through the application of innovative structural design, interconnection technology, materials, and equipment. It helps realize higher integration, better performance, smaller size, lower power consumption, and higher reliability of semiconductor. It is not only a key post-process in semiconductor manufacturing but also a core technical path to continue the improvement of semiconductor performance and meet the complex application demands of downstream industries against the background of the slowing down of Moore's Law.
- Due to the differences in electrical performance, size, application scenarios and other factors of different semiconductor products, the packaging forms are diverse and complex. According to whether there are a packaging substrate and the material of the packaging substrate, semiconductor packaging products can be divided into different categories. Among them, there are different packaging technologies in each category. The following presents the classification of typical packaging technologies.



Source: WSTS, SIA, Frost Sullivan Report

Overview of Global Advanced Packaging & Testing Market

Introduction of Typical Advanced Packaging Technologies

Packaging Technology	Packaging Structure	Technical Principle	Major Application
WLP (Fan-in)		Wafer-Level Packaging (Fan-In WLP) completes the packaging process directly on the wafer before dicing. Redistribution layers (RDLs) are formed through photolithography to reroute the chip pads, and solder bumps are created through ball planting. All I/O bumps are distributed within the original chip area, enabling direct interconnection between the die and the PCB. The final package size is nearly equal to that of the bare die.	Wearable devices, 5G RF modules, miniaturized sensors, and power devices.
WLP (Fan-out)		In Fan-out WLP, the diced chips are mounted on a temporary carrier and encapsulated with molding compound to form a reconstituted wafer. RDLs are then fabricated to extend the I/O pads beyond the chip area to a larger package surface. Without the need for a substrate, solder balls are formed directly on the reconstituted wafer. This structure breaks the limitation of the die area, enabling higher I/O density, more flexible layout, and multi-chip heterogeneous integration with high-density interconnection.	Smartphone application processors (APs), GPUs, RF chips, IoT devices, and automotive electronics.
BGA		BGA packages use a substrate as an interposer. The chip is interconnected to the substrate via wire bonding or flip-chip soldering. Solder balls are arranged in an array on the bottom of the substrate, providing both electrical and mechanical connections to external circuits such as PCBs through reflow soldering. This structure is well suited for devices with high pin counts.	Computer processors, image processing chips, networking processors, and consumer SoCs.

Overview of Global Advanced Packaging & Testing Market

Introduction of Typical Advanced Packaging Technologies

Packaging Technology	Packaging Structure	Technical Principle	Major Application
LGA		LGA packages also employ a substrate as the interposer, with the die connected to it through wire bonding or flip-chip methods. A grid of metallic pads is placed on the bottom of the substrate, enabling electrical connection to external circuitry such as PCBs. LGA offers high integration density, compact form factor, and excellent design flexibility.	5G communication modules, mobile terminals, IoT devices, and microcontrollers (MCUs).
Flip-Chip QFN		FC-QFN utilizes a metal lead frame as the interconnection medium. The chip is mounted onto the frame through flip-chip soldering, and flat pads on the bottom of the frame enable electrical connection with PCBs or other circuits. The package features low cost, high reliability, and good thermal performance.	Consumer electronics, IoT modules, industrial MCUs, and automotive chips.
2.5D		2.5D integration uses an interposer—typically containing through-silicon vias (TSVs), through-glass vias (TGVs), or organic RDL interposers—as an interconnection bridge to integrate multiple dies side by side. Homogeneous or heterogeneous chips achieve high-speed communication through ultra-dense wiring within the interposer, which is then connected to the substrate. This approach enables extremely high interconnect density and bandwidth without vertically stacking the dies.	AI accelerators, GPU + HBM integration, high-end FPGAs, and network processors.
3D		3D packaging vertically stacks multiple dies using through-silicon vias (TSVs), micro-bumps, and advanced bonding technologies such as TCB (Thermal Compression Bonding) or Hybrid Bonding. This achieves direct electrical connection between stacked dies, significantly shortening interconnect paths and improving integration density as well as data transmission efficiency.	Mobile processors, HBM memory, AI chips, and stacked GPUs.

Overview of Global Advanced Packaging & Testing Market

Introduction to the Merits of Semiconductor Advanced Packaging

- Traditional packaging: Its main functions are semiconductor protection, size enlargement, and electrical connection. It connects the chip with external circuits through methods such as wire bonding and provides mechanical protection and heat dissipation.
- Advanced packaging: On the basis of traditional packaging, it adds the functions of improving functional density, shortening interconnection length, and performing system reconstruction. It can increase product integration and functional diversification without relying on breakthroughs in chip manufacturing processes.

Comparison Between Advanced Packaging and Traditional Packaging

Packaging Type	Traditional Packaging	Advanced Packaging	
Technology Type	Leadframe wire-bond	BGA	2.5D/3D
System Memory Bandwidth	Low	Medium	High
Chip Power Ratio	Low	Medium	High
Chip Size	Large	Small	Small
Heat Dissipation Efficiency	Low	High	High
Packaging Cost	Low	Medium	High
Performance	Low	Medium	High
Packaging Form	With lead frames as the carrier, chip and external pins are connected unidirectionally through wire bonding. The package size is much larger than the chip, and the number of pins is small and distributed sparsely.	By means of Redistribution Layer (RDL), interposer or vertical stacking structure, technologies such as flip-chip bonding and Through-Silicon Via (TSV) are adopted to realize high-density interconnection of multiple chips. The package size is close to the chip, and the integration degree and performance are greatly improved.	
Global Demand	2020-2025: 7.7%	2020-2025: 13.1%	
Growth Rate	2025-2030E: 7.8%	2025-2030E: 14.8%	

Overview of Global Semiconductor Packaging & Testing Market

Global Semiconductor Advanced Packaging & Testing Market Size (1/2)

- Driven by the demand for high-integration and low-power consumption chips in the fields of communications, consumer electronics, high-performance computing, and artificial intelligence, the market scale of the advanced semiconductor packaging and testing industry—backed by technologies such as flip-chip bonding, wafer-level packaging, and 2.5D/3D packaging — has achieved rapid growth, emerging as one of the segments with leading growth rates in the semiconductor industry chain. The global market size increased from RMB214.1 billion in 2020 to RMB396.7 billion in 2025, with a CAGR of 13.1%.
- Over the next five years, as Moore's Law slows down, advanced packaging and testing—serving as a core path to enhance chip performance—will further benefit from the popularization of autonomous driving, data centers, high-performance computers, and smart wearable devices, as well as the maturity of cutting-edge packaging and testing technologies. It will maintain a robust growth momentum, with its market scale expected to expand steadily. In 2025, the global advanced packaging and testing market accounted for more than 50% of the overall packaging and testing market for the first time, surpassing traditional packaging. By 2030, the global advanced packaging market scale is expected to reach RMB790.3 billion, with a CAGR of 14.8% from 2025 to 2030. In contrast to traditional packaging, which features relatively low added value and a saturated market, advanced packaging boasts high technical barriers and supply scarcity. Its unit price and demand growth rate are significantly higher, enabling its market scale to outperform the overall packaging and testing industry in terms of growth rate over the long term.
- The PRC market has delivered outstanding performance. Although the PRC still lags behind some overseas markets in advanced packaging and testing technologies, Chinese enterprises have made aggressive investments in advanced packaging and testing technologies and production capacity scale to meet the rapidly growing downstream demand. The market size of advanced packaging and testing in the PRC increased to RMB126.2 billion in 2025, with a CAGR of 16.6% from 2020 to 2025. It is projected that by 2030, the relevant market size will further grow to RMB298.5 billion, with a CAGR of 18.8% — significantly higher than the global average growth rate.

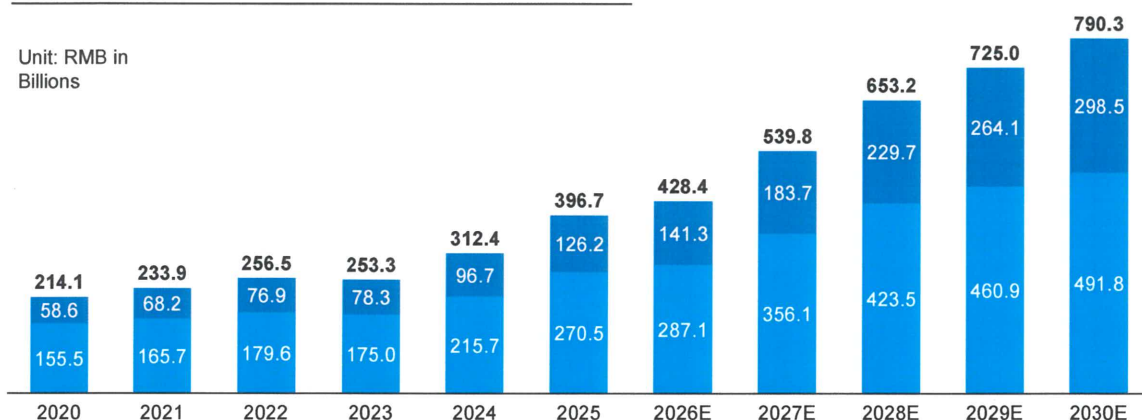
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Global Semiconductor Advanced Packaging & Testing Market Size

Global and China Semiconductor Advanced Packaging & Testing Market Size

	CAGR	2020-2025	2025-2030E
PRC*		16.6%	18.8%
Rest of the World		11.7%	12.7%
Global		13.1%	14.8%

Unit: RMB in Billions



Source: Expert Interview, Frost & Sullivan

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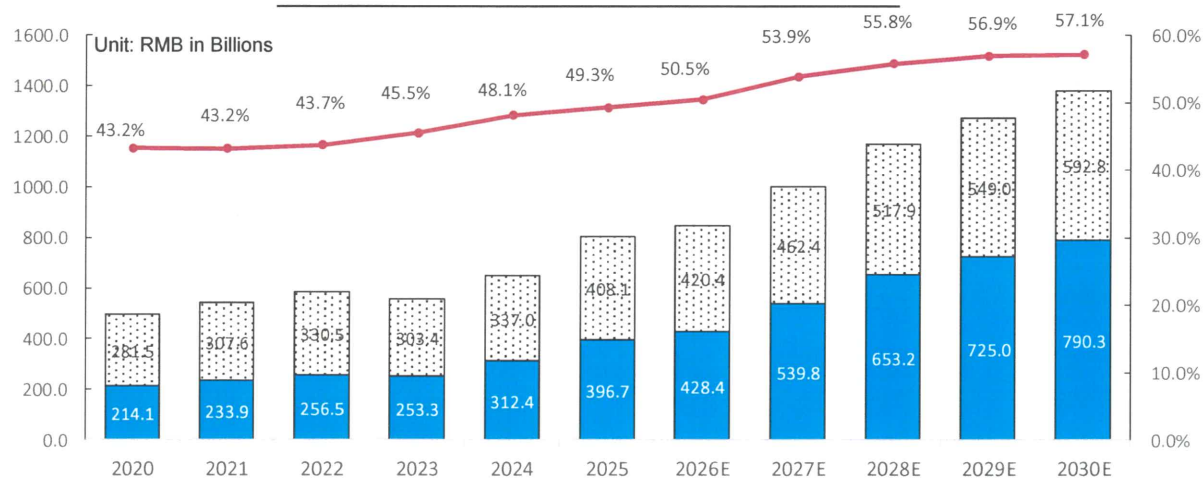
Overview of Global Semiconductor Packaging & Testing Market

Penetration of Global Semiconductor Advanced Packaging & Testing

Global Semiconductor Advanced Packaging & Testing Market Size and Penetration

Traditional P&T Advanced P&T Penetration Rate

	CAGR	2020-2025	2025E-2030E
Advanced P&T		13.1%	14.8%
Traditional P&T		7.7%	7.8%
Total		10.2%	11.4%



Source: Expert Interview, Frost & Sullivan

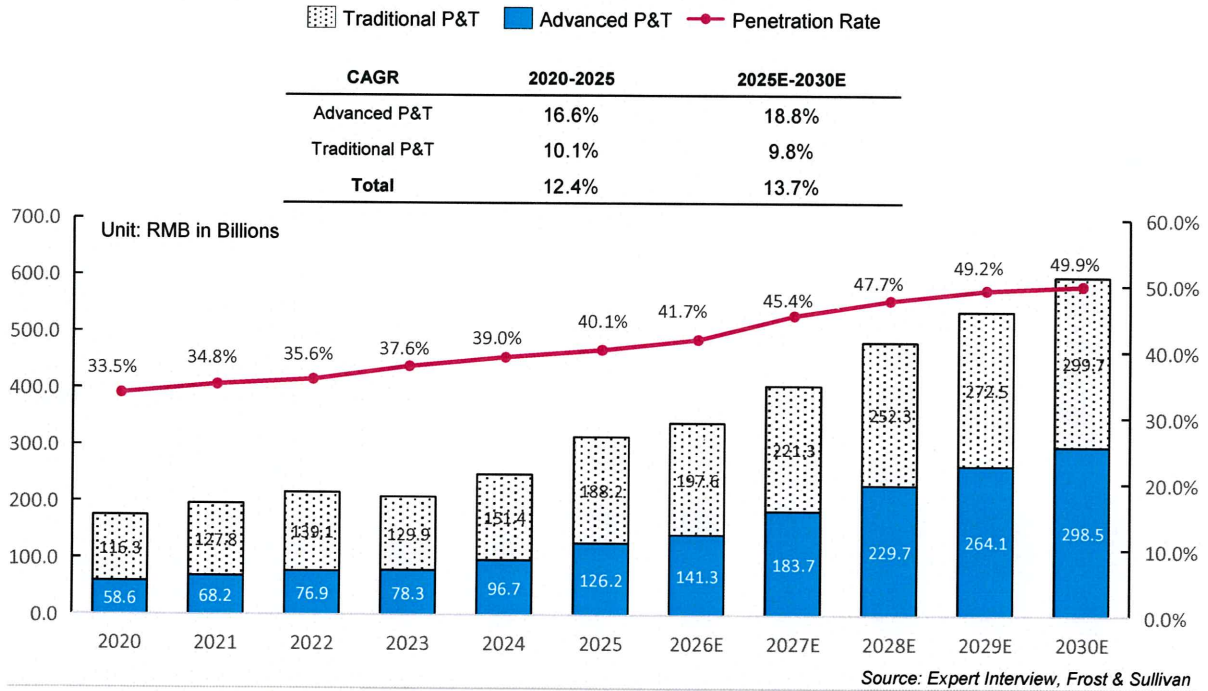
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Overview of Global Semiconductor Packaging & Testing Market

Penetration of Chinese Mainland Semiconductor Advanced Packaging & Testing

Chinese Mainland Semiconductor Advanced Packaging & Testing Market Size and Penetration



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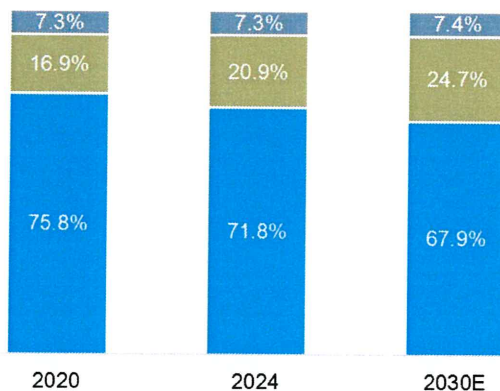
2024 ADVANCED PACKAGING REVENUE SPLIT

Market Shares by End Market

From 2020 to 2030, the advanced packaging revenue share is undergoing a significant shift. The Mobile & Consumer segment, while remaining the largest, is steadily declining from 75.8% in 2020 to a projected 67.8% in 2030. Conversely, the Telecom & Infrastructure sector demonstrates the strongest growth, expanding from 16.9% to 24.7% over the same period. The Automotive, Industrial, and other markets category remains relatively stable but is gradually increasing its share from 7.3% to 7.5%.

Market Share of Advanced Packaging Market, by Revenue of End Market, 2020-2030E

■ Mobile & Consumer ■ Telecom & Infrastructure ■ Others



- The Mobile & Consumer segment remains the largest market driver, but its share is declining from 75.8% in 2020 to a projected 67.8% in 2030. This shift reflects slower relative growth as the market matures, though absolute revenue remains strong due to continued high demand for smartphones, tablets, and IoT devices.
- In contrast, the Telecom & Infrastructure sector is growing fast, increasing its share from 16.9% to 24.7%. This expansion is driven by 5G deployment, data center scaling, and AI applications, which require high-performance advanced packaging such as 2.5D/3D IC and fan-out technologies.
- The Automotive, Industrial, and other markets category remains stable, with a slight share increase from 7.3% to 7.5%.

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Overview of Global Semiconductor Packaging & Testing Market

Drivers of Global Semiconductor Advanced Packaging & Testing Market (1/2)



High-performance Memory

The explosive growth of data volume and AI's demand for high bandwidth have driven the upgrading of storage packaging. 3D NAND breaks through stacking layer limits via TSV (Through-Silicon Via) technology to increase storage capacity; HBM (High Bandwidth Memory) co-packaging evolves toward HBM3/HBM3e to reduce data transmission latency. Combined with thermal management processes, it meets the high-speed read-writerequirements of AI scenarios.



Data Center and High-Power Computing (HPC)

Against the backdrop of exponential data center traffic growth, demands for computing power and data transmission efficiency have jointly driven advanced packaging innovation. On the computing side, AI large models and HPC's need for higher computing power and energy efficiency has led advanced packaging to integrate multiple chiplets via Chiplet heterogeneous integration — boosting computing density while solving heat issues with thermal management. On the optoelectronic side, to adapt to 800G/1.6T high-speed, low-power optical module evolution, advanced packaging optimizes the collaborative process between optoelectronic devices and chips. Technologies like FanOut and TSV reduce optoelectronic interface signal loss, enabling seamless synergy between computing chips and optical components to meet data centers' ultra-low latency and high-bandwidth needs.



Automotive Electronics

The upgrading of intelligent driving and popularization of V2X (Vehicle-to-Everything) require automotive chips to have high integration and reliability. Advanced packaging adopts temperature-resistant and vibration-resistant materials as well as SiP (System-in-Package) technology, integrates various chips and enhances EMC (Electromagnetic Compatibility) design to ensure stable operation in complex automotive environments.

Overview of Global Semiconductor Packaging & Testing Market

Drivers of Global Semiconductor Advanced Packaging & Testing Market (2/2)



Consumer Electronics

As terminal devices upgrade toward being thinner, lighter and lower-power, WLP (including Fan-in and Fan-out) technologies reduce packaging size. At the same time, heterogeneous integration is used to integrate multiple modules, balancing power consumption and functional richness to adapt to devices such as foldable screens and AR/VR (Augmented Reality/Virtual Reality) products.



Industrial Electronics

The industrial internet drives chips to transform toward high computing power and high stability. Advanced packaging adopts high-reliability interconnection processes and protective materials, and improves integration via 2.5D/3D packaging. It supports real-time data processing to meet the long-term stable operation requirements of industrial equipment.

Overview of Global Semiconductor Packaging & Testing Market

Trends of Global Semiconductor Advanced Packaging & Testing Market

Multi-sector demand fuels advanced packaging and testing market.

The semiconductor advanced packaging and testing market is largely driven by its diverse applications across sectors like high-performance memory, data centers, automotive, and consumer electronics. Technologies like 3D NAND and HBM address AI and data volume demands, while data centers leverage Chiplet heterogeneous integration for better computing power and energy efficiency. Automotive and consumer electronics require compact, reliable, and efficient solutions, further fueling the adoption of advanced packaging. In the consumer electronics sector, global XR (Extended Reality) device shipments reached approximately 14.5 million units in 2025, representing a year-on-year increase of 44.4%. XR devices use application processors, memory chips, display driver ICs, sensor chips and connectivity chips for computing, image display, spatial sensing and wireless connectivity, while their compact form factors require high-density chip integration. In the automotive electronics sector, NEV sales in China reached approximately 16.5 million units in 2025, representing a year-on-year increase of 28.2%. Semiconductors are widely used in NEVs for battery management, power control, advanced driver-assistance systems and in-vehicle infotainment systems, with increasing vehicle electrification and intelligence also raising requirements for packaging performance and reliability.

Rising status of the packaging segment in the industrial chain.

As semiconductor process technologies hit physical limits, advanced packaging's role in system-level integration and performance enhancement has become increasingly vital. It is no longer just about chip protection or connection, but a key strategy for companies to boost competitiveness and meet emerging semiconductor needs.

Advanced Packaging Technologies Moving Further Toward High Performance and Miniaturization.

With end applications demanding better electronic product performance and smaller sizes, advanced packaging/testing technologies are inevitably evolving toward high performance and miniaturization. For example, 2.5D/3D packaging uses silicon interposers or through-silicon vias (TSVs) for vertical chip interconnection, significantly improving integration and signal speed to serve high-computing scenarios like AI and data center chips. Wafer-level packaging (WLP), meanwhile, reduce size and space occupation, ideal for consumer electronics such as smartphones and wearables. This trend will deepen to break existing technical bottlenecks.

Overview of Global Semiconductor Packaging & Testing Market

Trends of Global Semiconductor Advanced Packaging & Testing Market

Accelerating Localization Trend in Advanced Packaging and Testing.

Driven by changing international trade environments and PRC's demand for independent semiconductor development, localization in advanced packaging/testing has become more prominent. Domestic enterprises have made continuous breakthroughs in advanced packaging technology; in equipment, though high-end localization remains low, domestic manufacturers are ramping up efforts, with some products already achieving localized replacement. As R&D, talent cultivation, and capital investment increase, the localization process will further accelerate.

Supportive government policies.

The "Opinions on Deepening the Implementation of the Artificial Intelligence Plus Action" target an application penetration rate of over 70% for new-generation intelligent terminals and intelligent agents by 2027. The expansion of AI applications is expected to increase demand for high-performance semiconductors and advanced packaging and testing. Other policies, including the "Several Policies for Promoting the High-quality Development of the Integrated Circuit and Software Industries in the New Era" and the relevant 2025 notice, provide tax and other support to eligible integrated circuit enterprises, including advanced packaging and testing enterprises, thereby supporting industry development and creating market opportunities for the Group.

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- 1 Introduction of the Research
- 2 Overview of Global Semiconductor Market
- 3 Overview of Global Packaging & Testing Market
- 4 Overview of Global Advanced Packaging Market
- 5 Competitive Global Landscape of Packaging & Testing Market
- 6 Appendix

Competitive Landscape of Packaging & Testing Market

Introduction of Top Players in Chinese Mainland Market

- There are a large number of participants in PRC's semiconductor packaging and testing market, with approximately 150 to 200 OSATs. Most of these OSATs are mainly engaged in traditional packaging and testing businesses. They generally have small overall revenue scales, and the proportion of revenue from advanced packaging and testing in their total revenue is relatively low.
- In addition, affected by the wide variety of semiconductor products, two types of OSATs have been formed in the market, which are General-Purpose OSATs and Application-Specific OSATs. General-Purpose OSATs offer packaging and testing services for many different types of chips used in various fields. They do not focus on just one chip type; instead, they have flexible capabilities to serve a wide range of customer needs. Application-Specific OSATs specialize in packaging and testing only chips for specific uses. Their technologies and processes are tailored to meet the unique requirements of these niche fields, rather than serving all chip types and industries. In terms of the total revenue of semiconductor packaging and testing, our company ranked 7th in PRC's General-Purpose OSAT companies.
- In terms of the revenue in 2025, our Company ranked 7th among general-purpose semiconductor OSAT in PRC, with a market share of 0.6%.

Competitive Landscape of Packaging & Testing Market

Introduction of Top Players in Chinese Mainland Market

Ranking of China's OSAT Companies, 2025, by Revenue of Semiconductor Packaging and Testing

Unit: RMB in billions

Ranking	Company	P&T	P&T Share	Application-Specific / General-Purpose	Listed Status
1	Company A (长电科技)	38.7	12.3%	General-Purpose	Listed
2	Company B (通富微电)	27.3	8.7%	General-Purpose	Listed
3	Company C (华天科技)	17.2	5.5%	General-Purpose	Listed
4	Company D (智路封测)	16.5	5.2%	General-Purpose	Unlisted
5	Company E (盛合晶微)	6.7	2.1%	General-Purpose	Listed
6	Company F (甬矽电子)	4.3	1.4%	General-Purpose	Listed
7	Company J (沛顿科技)	3.6	1.1%	Application-Specific	Unlisted
8	Company K (太极实业)	2.9	0.9%	Application-Specific	Listed
9	Company L (宏茂微)	2.7	0.9%	Application-Specific	Unlisted
10	Company M (顾中科技)	2.2	0.7%	Application-Specific	Listed
11	Company N (新汇成)	1.6	0.5%	Application-Specific	Listed
12	Company O (晶方半导体)	1.2	0.4%	Application-Specific	Listed
13	The Company	1.0	0.3%	General-Purpose	Unlisted
14	Company H (华宇电子)	0.8	0.3%	General-Purpose	Listed
15	Company G (气派科技)	0.7	0.2%	General-Purpose	Listed
16	Company I (蓝箭电子)	0.4	0.1%	General-Purpose	Listed

Competitive Landscape of Packaging & Testing Market

Introduction of Top Players in Chinese Mainland Market

Ranking of China's OSAT Companies, 2025, by Revenue of Semiconductor Advanced Packaging and Testing

Unit: RMB in billions

Ranking	Company	Advanced P&T	Proportion of Advanced P&T Revenue	Advanced P&T Share	Application-Specific / General-Purpose	Listed Status
1	Company A (长电科技)	28.3	73%	22.4%	General-Purpose	Listed
2	Company B (通富微电)	19.6	72%	15.5%	General-Purpose	Listed
3	Company C (华天科技)	11.7	68%	9.3%	General-Purpose	Listed
4	Company D (智路封测)	8.8	53%	6.9%	General-Purpose	Unlisted
5	Company E (盛合晶微)	6.7	100%	5.3%	General-Purpose	Listed
6	Company F (甬矽电子)	2.7	61%	2.1%	General-Purpose	Listed
7	Company K (太极实业)	2.4	85%	1.9%	Application-Specific	Listed
8	Company M (顾中科技)	2.1	95%	1.6%	Application-Specific	Listed
9	Company J (沛顿科技)	2.0	55%	1.6%	Application-Specific	Unlisted
10	Company L (宏茂微)	1.9	68%	1.5%	Application-Specific	Unlisted
11	Company N (新汇成)	1.4	90%	1.1%	Application-Specific	Listed
12	Company O (晶方半导体)	1.0	90%	0.8%	Application-Specific	Listed
13	The Company	0.7	73%	0.6%	General-Purpose	Unlisted
14	Company G (气派科技)	0.3	40%	0.2%	General-Purpose	Listed

Competitive Landscape of Packaging & Testing Market

Introduction of Top Players in Chinese Mainland Market

Ranking of China's General-Purpose OSAT Companies, by Revenue of Semiconductor Advanced Packaging and Testing in 2025

Unit: RMB in billions

Ranking	Company	P&T	P&T Share	Advanced P&T	Proportion of Advanced P&T Revenue	Advanced P&T Share	Listed Status
1	Company A (长电科技)	38.7	12.3%	28.3	73%	22.4%	Listed
2	Company B (通富微电)	27.3	8.7%	19.6	72%	15.5%	Listed
3	Company C (华天科技)	17.2	5.5%	11.7	68%	9.3%	Listed
4	Company D (智路封测)	16.5	5.2%	8.7	53%	6.9%	Unlisted
5	Company E (盛合晶微)	6.7	2.1%	6.7	100%	5.3%	Listed
6	Company F (甬矽电子)	4.3	1.4%	2.7	61%	2.1%	Listed
7	The Company	1.0	0.3%	0.7	69%	0.6%	Unlisted
8	Company G (气派科技)	0.7	0.2%	0.3	40%	0.2%	Listed
9	Company H (华宇电子)	0.8	0.3%	0.2	26%	0.2%	Listed
10	Company I (华宇电子)	0.4	0.1%	0.1	28%	0.1%	Listed

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Competitive Landscape of Packaging & Testing Market

Introduction of Top Players in Chinese Mainland Market

Ranking of China's General-Purpose OSAT Companies, by Revenue of Semiconductor Traditional Packaging and Testing in 2025

Unit: RMB in billions

Ranking	Company	P&T	P&T Share	Traditional P&T	Traditional P&T Share	Listed Status
1	Company A (长电科技)	38.7	12.3%	10.45	5.6%	Listed
2	Company D (智路封测)	16.5	5.2%	7.76	4.1%	Unlisted
3	Company B (通富微电)	27.3	8.7%	7.63	4.1%	Listed
4	Company C (华天科技)	17.2	5.5%	5.51	2.9%	Listed
5	Company F (甬矽电子)	4.3	1.4%	1.68	0.9%	Listed
6	Company H (华宇电子)	0.8	0.3%	0.58	0.3%	Listed
7	Company G (气派科技)	0.7	0.2%	0.43	0.2%	Listed
8	The Company	1.0	0.3%	0.27	0.1%	Unlisted
9	Company I (蓝箭电子)	0.4	0.1%	0.26	0.1%	Listed

Competitive Landscape of Packaging & Testing Market

Introduction of Top Players in Chinese Mainland Market

Packaging Technology		The Company	Company A	Company B	Company C	Company D	Company E	Company F	Company H	Company M
2.5D/3D	FOCT-R/S/L	√	√	√	√	×	√	√	×	×
	TGV	√	√	√	√	×	√	×	×	×
WLP	Fan-out WLP	√	√	√	√	√	√	√	√	×
	Fan-in-WLP	√	√	√	√	√	√	√	√	×
	BUMPING	√	√	√	√	√	√	√	√	×
BGA	WB/FC-BGA	√	√	√	√	√	√	√	×	√
	Hybrid-BGA	√	√	√	√	√	×	√	×	×
LGA	WB/FC-LGA	√	√	√	√	√	×	√	×	√
	Hybrid-LGA	√	√	√	√	√	×	√	×	√
FC-QFN		√	√	√	√	√	×	√	×	√

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Competitive Landscape of Packaging & Testing Market

Entry Barriers of Semiconductor Advanced Packaging Industry

The PRC semiconductor packaging and testing market comprises approximately 150 to 200 OSATs, many of which primarily provide traditional packaging services. The barriers to establishing and sustaining advanced packaging operations principally relate to technological capabilities, capital investment and customer qualification. Their significance varies according to packaging technology, application and production scale.

➤ Technology and Process Capabilities.

Advanced packaging requires the integration of equipment, materials and manufacturing processes to meet customers' performance and reliability requirements. Commercial production also requires consistent yields, effective quality control and failure analysis capabilities. Developing these capabilities involves experienced engineering teams, process development, trial production and accumulated manufacturing experience. Purchasing equipment alone does not establish the process capabilities required for reliable volume production.

➤ Capital Investment and Production Scale.

OSATs require substantial investment in production premises, cleanrooms, packaging and testing equipment and supporting infrastructure, together with continuing expenditure on process development and equipment upgrades. The required investment varies by technology and capacity. Operators must also secure sufficient production volumes and utilisation to spread depreciation and other fixed costs, creating financial and operating challenges during production ramp-up.

➤ Customer Qualification and Operating Track Record.

Customers generally assess suppliers' quality systems, technical capabilities, product yields and reliability through audits, sample validation and trial production. Successful qualification, consistent delivery and a demonstrated production record support the conversion of initial orders into recurring business. New entrants therefore require both technical readiness and the ability to demonstrate reliable production performance to customers.

The relatively recent establishment of certain market participants does not necessarily indicate limited industry experience. Company D is an investment platform whose semiconductor packaging and testing business includes acquired operations with existing capabilities and operating histories. Company E was established with support from established semiconductor manufacturers, while Company F's core technical team had prior experience in the packaging and testing industry. Companies E and H were established in 2014 and Company F in 2017, allowing several years for capability development before 2025. These examples demonstrate that the barriers can be overcome through investment, experienced personnel, acquired capabilities and customer qualification.

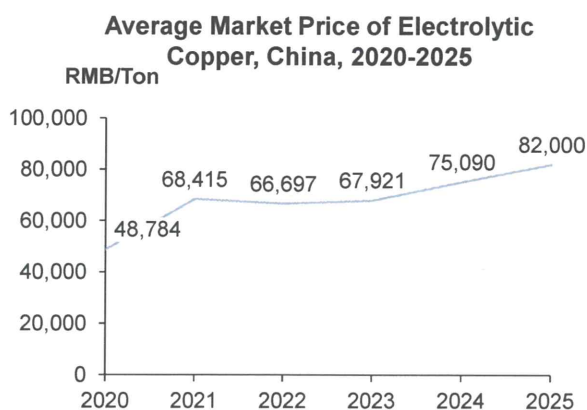
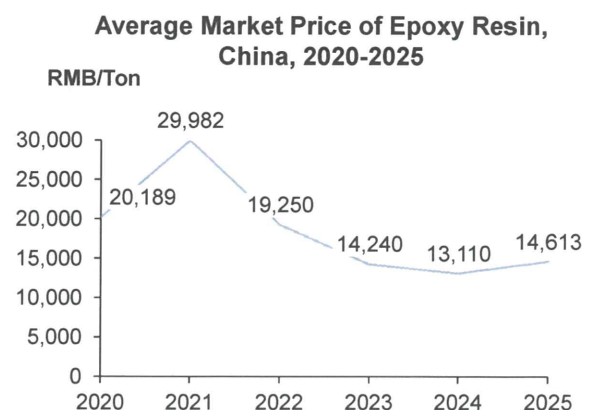
Cost Analysis

Average Market Price of Electrolytic Copper and Epoxy Resin

- Semiconductor packaging and testing is generally materials-intensive. Materials typically account for more than 50% of cost of sales, while the remaining cost base primarily consists of labor, depreciation, factory overhead and testing-related expenses. In substrate-based advanced packages such as FC-BGA, the IC substrate is often the largest single cost component and may account for approximately 50% of total packaging cost. Electrolytic copper and epoxy resin are two important upstream materials for IC substrates. Copper is mainly used in the form of electrolytic copper foil and plated copper structures for substrate wiring and interconnection, while epoxy-resin systems are widely applied in dielectric build-up films such as ABF and in resin systems for laminate materials. For ABF substrates, copper-linked inputs generally represent around 10% to 20% of substrate cost, while epoxy-resin-linked inputs generally represent around 25% to 35% of substrate cost.
- During 2020 to 2025, the average market price of electrolytic copper in China increased from RMB48,784 per ton to RMB82,000 per ton, representing a volatile but overall upward trend. The average market price further increased from RMB75,090 per ton in 2024 to RMB82,000 per ton in 2025, indicating continued cost pressure on copper-linked materials used in IC substrates. In contrast, the average market price of epoxy resin in China declined significantly after reaching RMB29,982 per ton in 2021, falling to RMB13,110 per ton in 2024, before increasing to RMB14,613 per ton in 2025. Despite the rebound in 2025, epoxy resin prices remained substantially lower than the 2021 peak.
- The combined impact of these price movements on semiconductor packaging and testing companies depends on their product mix, material consumption structure, procurement arrangements and cost pass-through ability. For companies with greater exposure to substrate-based advanced packaging, higher copper prices may increase pressure on copper foil, plating and interconnect-related costs. At the same time, the lower level of epoxy resin prices compared with the 2021 peak may partly alleviate the cost burden of resin-linked substrate materials. As a result, while copper price increases may place upward pressure on the cost of high-density IC substrates, the correction in epoxy resin prices provides some offsetting support for cost control.

Cost Analysis

Average Market Price of Electrolytic Copper and Epoxy Resin



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Competitor Profiles (1/2)

Competitor	Profile
Company A (长电科技)	Company A is a public company founded in 1972 and is listed on Shanghai Stock Exchange. It provides semiconductor chip manufacturing services with a focus on IC packaging, assembly and test solutions for automotive, high-performance computing, memory and consumer applications.
Company B (通富微电)	Company B is a public company founded in 1997 and is listed on Shenzhen Stock Exchange. It is an OSAT company that focuses on advanced packaging solutions for high-performance computing, automotive, memory and other applications.
Company C (华天科技)	Company C is a public company founded in 2003 and is listed on Shenzhen Stock Exchange. It provides IC packaging and testing services for consumer, industrial, and automotive semiconductor products.
Company D (智路封测)	Company D is a private company founded in 2017 and is headquartered in Beijing. It provides packaging and testing services across discrete, analog, RF and other chip segments.
Company E (盛合晶微)	Company E is a private company founded in 2014 and is headquartered in Jiangsu Province. It specializes in wafer-level advanced packaging, multi-die chiplet integration, and related services for semiconductor products.
Company F (甬矽电子)	Company F is a public company founded in 2017 and is listed on Shanghai Stock Exchange. It provides IC packaging and test services with emphasis on advanced packaging technologies.

Appendix

Competitor Profiles (2/2)

Competitor	Profile
Company G (气派科技)	Company G is a public company founded in 2006 and is listed on Shanghai Stock Exchange. It is an advanced-packaging service provider.
Company H (华宇电子)	Company H is a public company founded in 2014 and is listed on the National Equities Exchange and Quotations. It provides packaging and testing services for integrated circuits.
Company I (蓝箭电子)	Company I is a public company founded in 1998 and is listed on the Shenzhen Stock Exchange. It provides packaging and testing services for discrete semiconductor devices and integrated circuits.
Company J (沛顿科技)	Company J is a private company founded in 2004 and is headquartered in Shenzhen. It provides chip back-end services including wafer thinning/grinding, die attach, wire-bond/flip-chip assembly, moulding and final test for a range of semiconductor customers.
Company K (太极实业)	Company K is a public company founded in 1966 and is listed on Shanghai Stock Exchange. Although diversified, the company includes semiconductor businesses as one of its core lines alongside other industrial operations.
Company L (宏茂微)	Company L J is a private company founded in 2002 and is headquartered in Shanghai. It supplies IC packaging and test services with a particular track record in memory packaging/test and automotive-grade quality systems.
Company M (颀中科技)	Company M is a public company founded in 2018 and is listed on Shanghai Stock Exchange and is headquartered in Hefei. It provides one-stop advanced packaging & testing services for customers in advanced packaging segments.
Company N (新汇成)	Company N is a public company founded in 2015 and is listed on Shanghai Stock Exchange. It provides integrated circuit packaging and testing services and has developed mid-to-high-end packaging capabilities since its founding.
Company O (晶方半导体)	Company O is a public company founded in 2005 and is listed on Shanghai Stock Exchange. It is a leading wafer-level CSP/WLCSP advanced-packaging specialist, especially known for image-sensor and sensor WLP solutions and large-scale wafer-level production.

F R O S T & S U L L I V A N

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Appendix

Supplementary Materials

- The Group's Advanced Packaging portfolio comprises BGA, LGA, WLP, 2.5D/3D, as well as FC-QFN and FC-SOT, while its Traditional Packaging offerings include WB-QFN.
- During the Track Record Period, revenue from Advanced Packaging amounted to RMB346.9 million, RMB587.2 million and RMB737.4 million in 2023, 2024 and 2025, respectively, while revenue from Traditional Packaging amounted to RMB161.5 million, RMB236.5 million and RMB271.2 million, respectively.
- From an industry perspective, lifecycle stage and market maturity are assessed by the breadth of commercial adoption, process standardization and extent of volume production. WB-QFN, BGA and LGA are mature and established technologies in both the global and PRC markets. WB-QFN remains a mainstream rather than obsolete or legacy technology, while advanced BGA and LGA variants continue to evolve. WLP is established and growing in both markets: fan-in WLP and WLCSP are mature, while fan-out and higher-density variants remain growth technologies. FC-QFN is commercially established and growth-stage globally; in the PRC, FC-QFN is in the growth stage. 2.5D/3D is in the commercial growth stage globally and the early growth stage in the PRC, where large-scale commercial capacity remains relatively limited.

